ANALOG DEVICES

Precision, 500 ns Settling BiFET Op Amp

AD744

FEATURES

AC PERFORMANCE

500 ns Settling to 0.01% for 10 V Step
1.5 μs Settling to 0.0025% for 10 V Step
75 V/μs Slew Rate
0.0003% Total Harmonic Distortion (THD)
13 MHz Gain Bandwidth – Internal Compensation
>200 MHz Gain Bandwidth (G = 1000) External Decompensation
>1000 pF Capacitive Load Drive Capability with 10 V/μs Slew Rate – External Compensation

DC PERFORMANCE

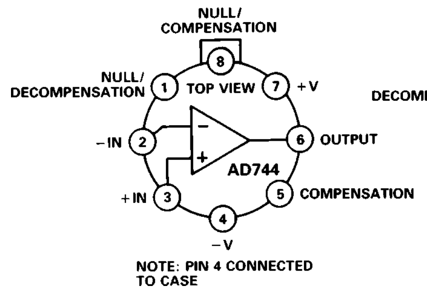
0.25 mV max Offset Voltage (AD744C)
3 μV/°C max Drift (AD744C)
250 V/mV min Open-Loop Gain (AD744B)
4 μV p-p max Noise, 0.1 Hz to 10 Hz (AD744C)
Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
MIL-STD-883B Processing Available
Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

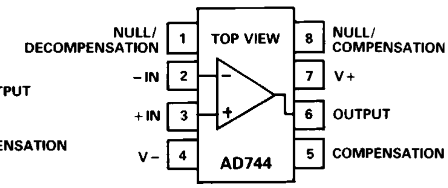
Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

CONNECTION DIAGRAMS

TO-99 (H) Package



8-Pin Plastic Mini-DIP (N)
8-Pin SOIC (R) Package and
8-Pin Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13 MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000 pF capacitive loads, slewing at 10 V/μs with full stability.

Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200 MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0°C to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of –40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of –55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin small outline, 8-pin cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OPA602/OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ionimplanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4 μV p-p, 0.1 Hz to 10 Hz (AD744C).

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD744–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	Typ	Max	AD744K/B/T Min	Typ	Max	AD744C Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	T_{MIN} to T_{MAX}			2/2/**2**			**1.0**			**0.45**	mV
vs. Temp.			5	20/20/**20**		5	**10**		2	**3**	μV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs. Supply	T_{MIN} to T_{MAX}	82/82/**82**			**88**			**92**			dB
Long-Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		30	**100**		30	**100**		30	**50**	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1.9	6.4		1.9	6.4		1.9	3.2	nA
S, T	125°C		31	102		31	102				nA
Either Input	V_{CM} = +10 V		40	150		40	**150**		40	**100**	pA
Offset Current	V_{CM} = 0 V		20	**50**		10	**50**		10	**20**	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V										
J, K	70°C		0.4	1.1		0.2	1.1				nA
A, B, C	85°C		1.3	3.2		0.6	3.2		0.6	1.3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = –1	8	13		9	13		9	13		MHz
Full Power Response	V_O = 20 V p-p		1.2			1.2			1.2		MHz
Slew Rate, Unity Gain	G = –1	**45**	75		**50**	75		**50**	75		V/μs
Settling Time to 0.01%[4]	G = –1		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic	f = 1 kHz										
Distortion	R1 ≥ 2 kΩ										
	V_O = 3 V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5.5		Ω‖pF
Common Mode			3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5.5		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		V
Over Max Operating Range[6]		**–11**		**+13**	**–11**		**+13**	**–11**		**+13**	V
Common-Mode											
Rejection Ratio	V_{CM} = ±10 V	**78**	88		**82**	88		**86**	94		dB
	T_{MIN} to T_{MAX}	76/76/**76**	84		**80**	84		**86**	90		dB
	V_{CM} = ±11 V	**72**	84		**78**	84		**80**	90		dB
	T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2			2	**4**	μV p-p
	f = 10 Hz		45			45			45		nV/√Hz
	f = 100 Hz		22			22			22		nV/√Hz
	f = 1 kHz		18			18			18		nV/√Hz
	f = 10 kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[7]	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	**200**	400		**250**	400		**250**	400		V/mV
	T_{MIN} to T_{MAX}	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current	Short Circuit		25			25			25		mA
Capacitive Load[8]	Gain = –1			**1000**			**1000**			**1000**	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			3.5	**5.0**		3.5	**4.0**		3.5	**4.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]PSRR test conditions: $+V_S$ = 15 V, $–V_S$ = –12 V to –18 V and $+V_S$ = +12 V to +18 V, $–V_S$ = –15 V.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –1, R_L = 2 k, C_L = 10 pF, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[6]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for C_{COMP} = 20 pF with the device connected as shown in Figure 32. Under these conditions, slew rate = 14 V/μs and 0.01% settling time = 1.5 μs typical. Refer to Table II for optimum compensation while driving a capacitive load.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . 500 mW
Input Voltage[3] . . . . ±18 V
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD744J/K . . . . 0°C to +70°C
  AD744A/B/C . . . . –40°C to +85°C
  AD744S/T . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
  8-Pin Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/Watt
  8-Pin Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 22°C/Watt
  8-Pin Metal Can Package: θ_{JA} = 150°C/Watt, θ_{JC} = 65°C/Watt
  8-Pin SOIC Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

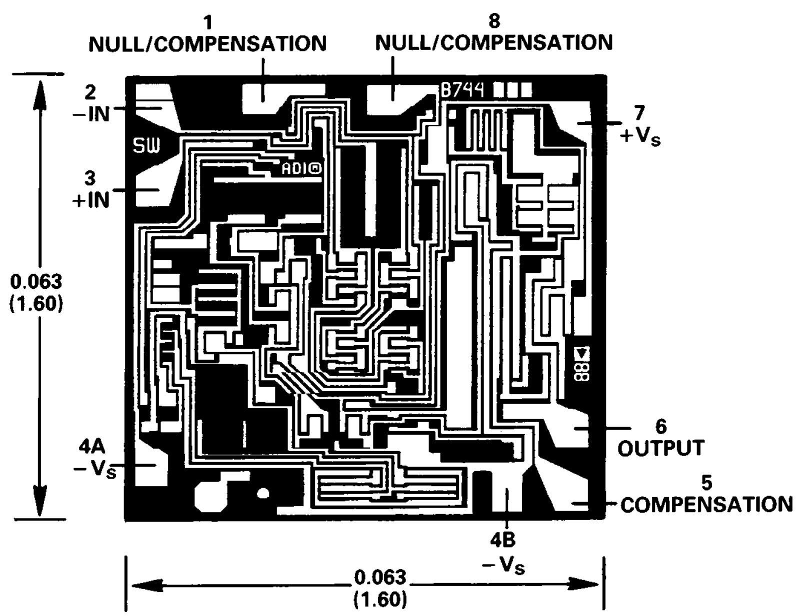
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD744JN	0°C to +70°C	N-8
AD744KN	0°C to +70°C	N-8
AD744JR	0°C to +70°C	R-8
AD744KR	0°C to +70°C	R-8
AD744AQ	–40°C to +85°C	Q-8
AD744BQ	–40°C to +85°C	Q-8
AD744CQ	–40°C to +85°C	Q-8
AD744AH	–40°C to +85°C	H-08A
AD744JChips	0°C to +70°C	Die
AD744JR-REEL	0°C to +70°C	Tape & Reel
AD744KR-REEL	0°C to +70°C	Tape & Reel

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip; H = TO-99 Metal Can.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD744–Typical Characteristics

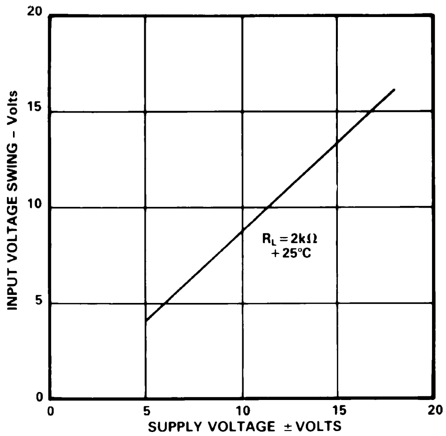


Figure 1. Input Voltage Swing vs. Supply Voltage

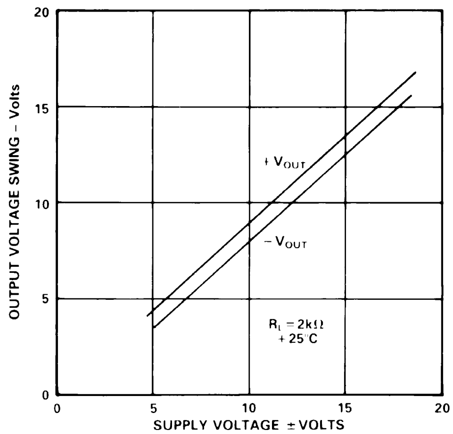


Figure 2. Output Voltage Swing vs. Supply Voltage

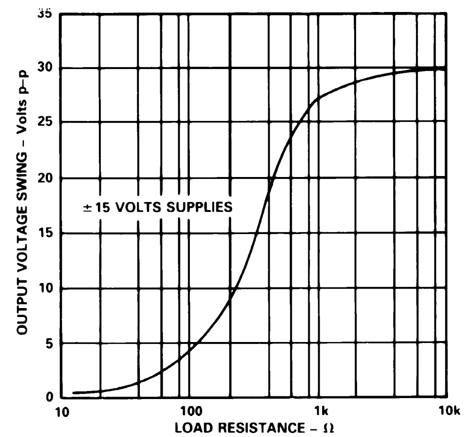


Figure 3. Output Voltage Swing vs. Load Resistance

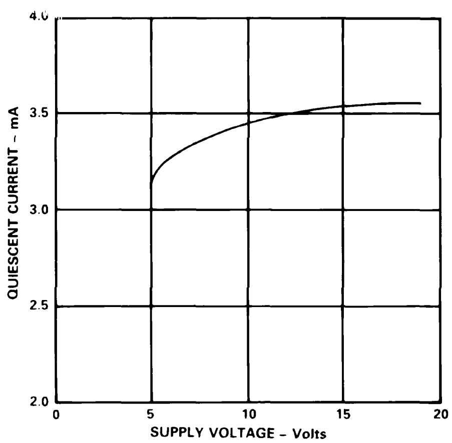


Figure 4. Quiescent Current vs. Supply Voltage

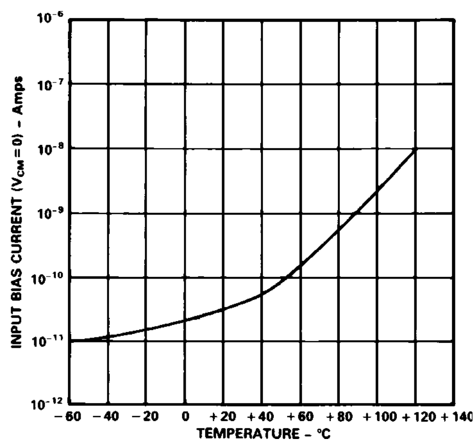


Figure 5. Input Bias Current vs. Temperature

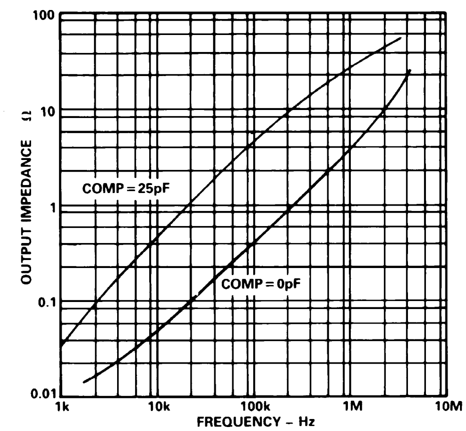


Figure 6. Output Impedance vs. Frequency

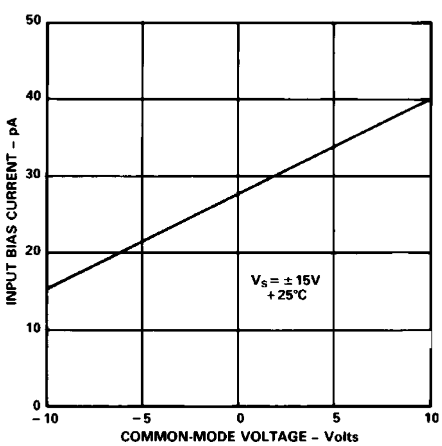


Figure 7. Input Bias Current vs. Common-Mode Voltage

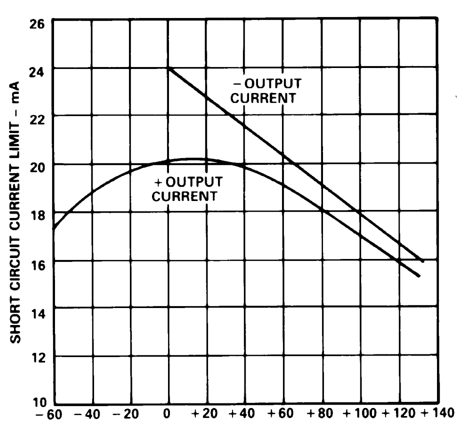


Figure 8. Short Circuit Current Limit vs. Temperature

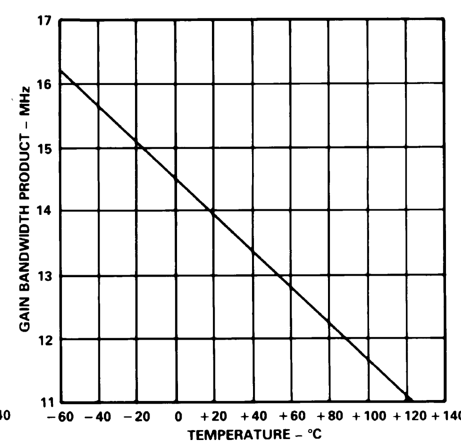


Figure 9. Gain Bandwidth Product vs. Temperature

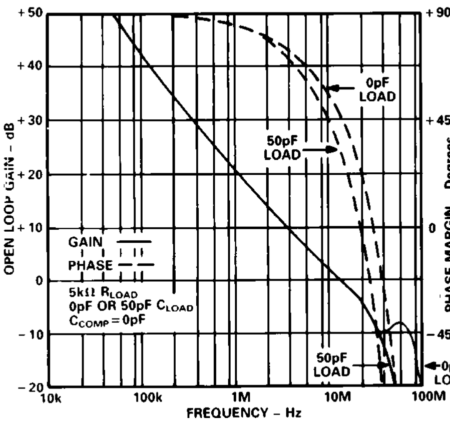


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency C_{COMP} = 0 pF

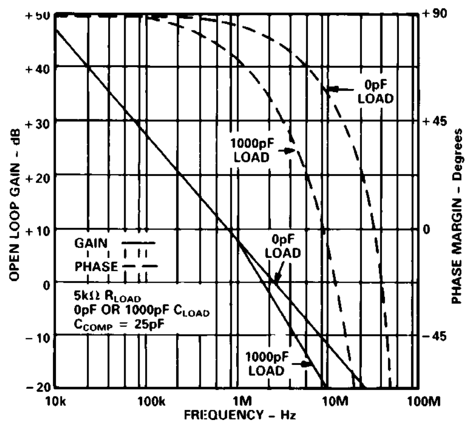


Figure 11. Open Loop Gain and Phase Margin vs. Frequency C_{COMP} = 25 pF

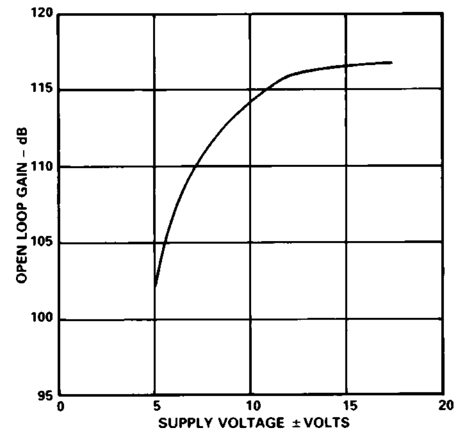


Figure 12. Open-Loop Gain vs. Supply Voltage

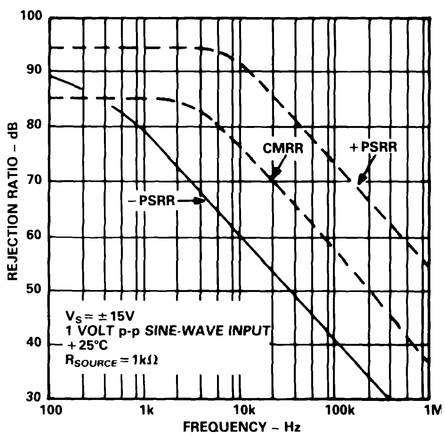


Figure 13. Common-Mode and Power Supply Rejection vs. Frequency

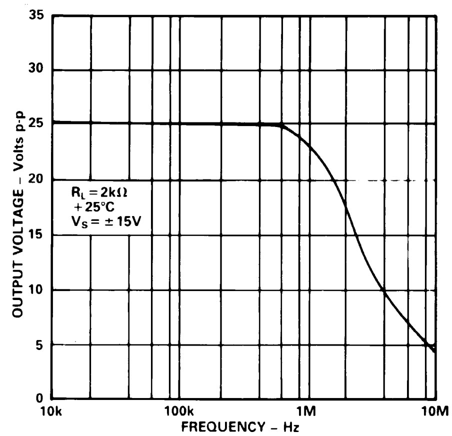


Figure 14. Large Signal Frequency Response

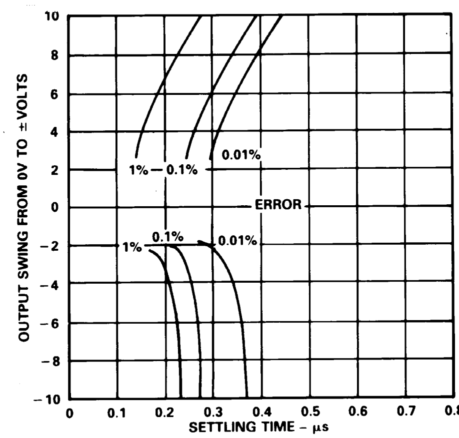


Figure 15. Output Swing and Error vs. Settling Time

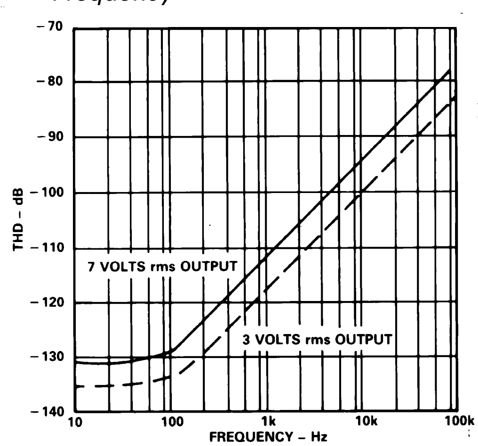


Figure 16. Total Harmonic Distortion vs. Frequency, Circuit of Figure 20 (G = 10)

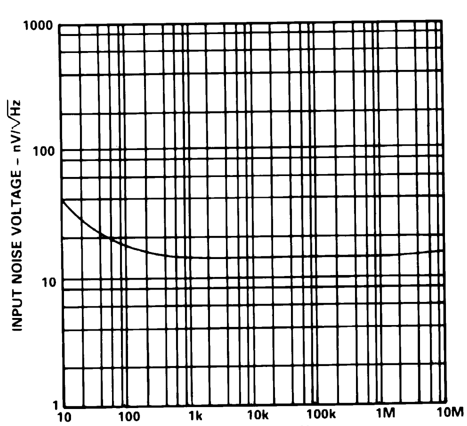


Figure 17. Input Noise Voltage Spectral Density

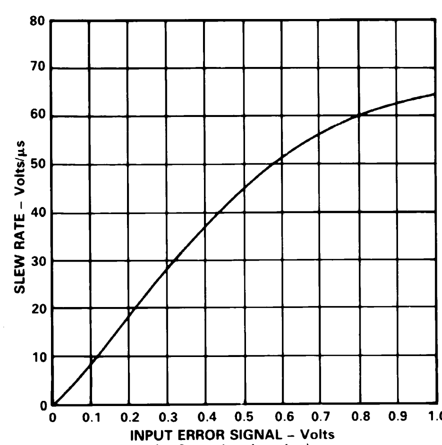


Figure 18. Slew Rate vs. Input Error Signal

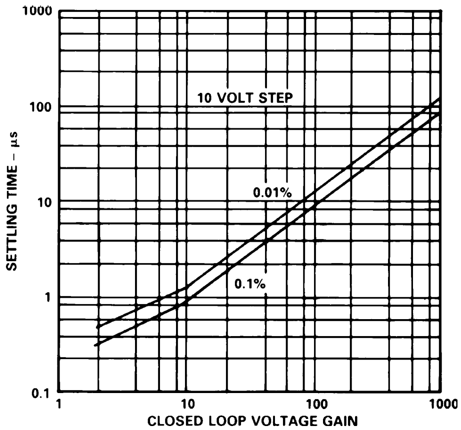


Figure 19. Settling Time vs. Closed Loop Voltage Gain

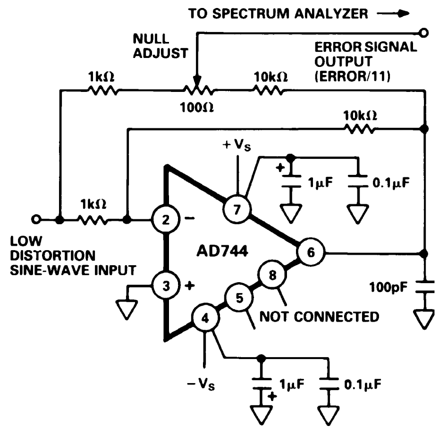


Figure 20. THD Test Circuit

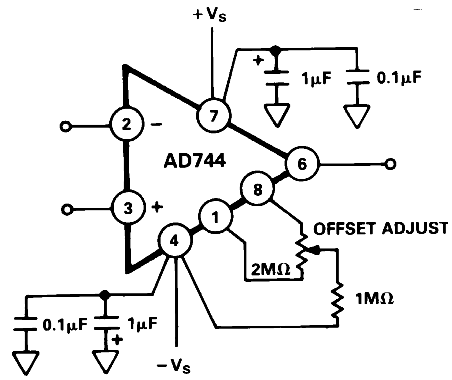


Figure 21. Offset Null Configuration

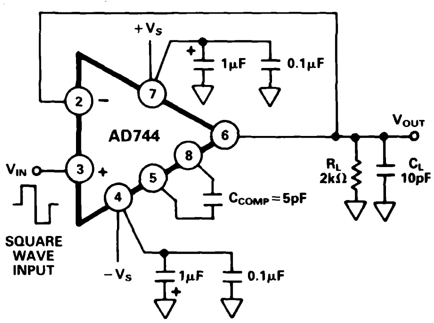


Figure 22a. Unity-Gain Follower

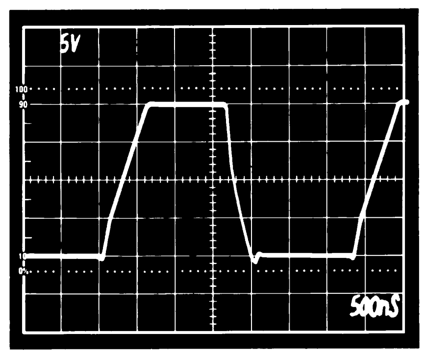


Figure 22b. Unity-Gain Follower Large Signal Pulse Response, C_{COMP} = 5 pF

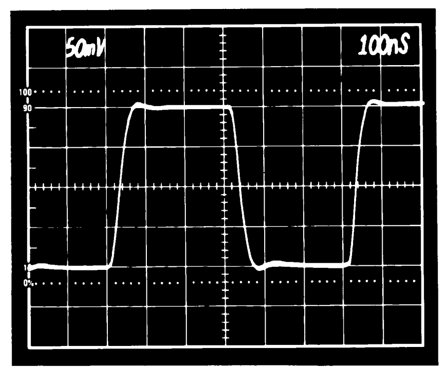


Figure 22c. Unity-Gain Follower Small Signal Pulse Response, C_{COMP} = 5 pF

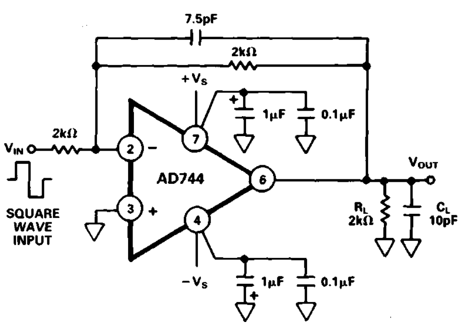


Figure 23a. Unity-Gain Inverter

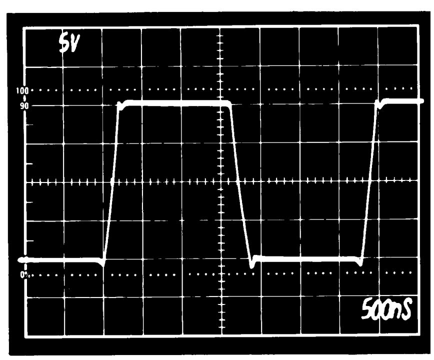


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response, C_{COMP} = 5 pF

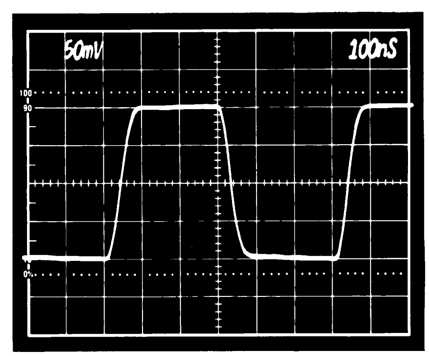


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response, C_{COMP} = 0 pF

POWER SUPPLY BYPASSING

The power supply connections to the AD744 must maintain a low impedance to ground over a bandwidth of 10 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 µF ceramic and a 1 µF electrolytic capacitor as shown in Figure 24 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 µF should be used for any application.

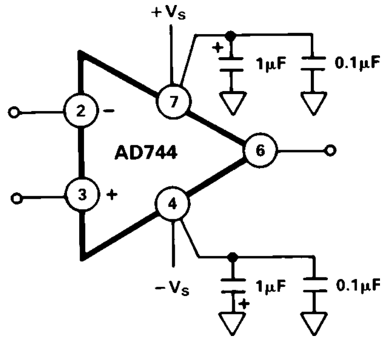


Figure 24. Recommended Power Supply Bypassing

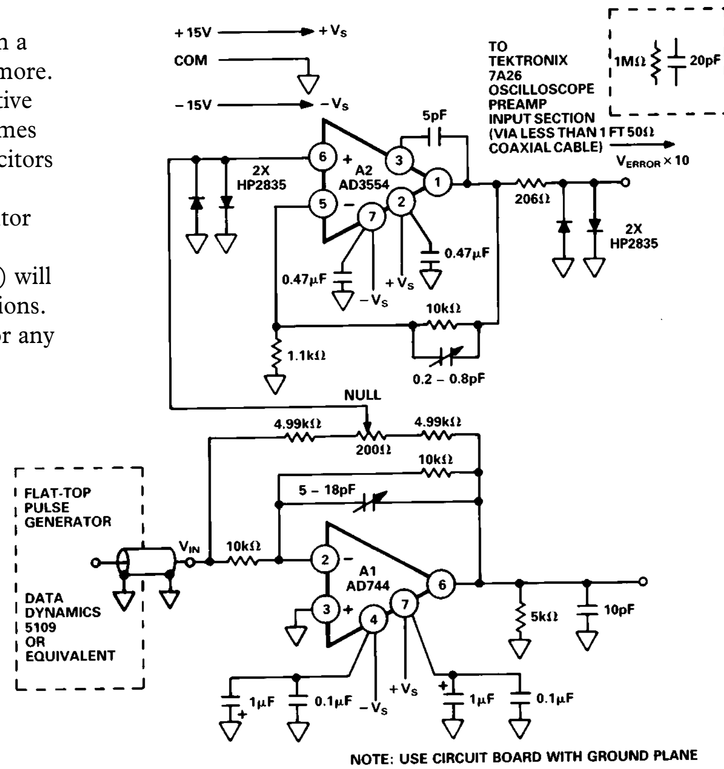


Figure 25. Settling Time Test Circuit

MEASURING AD744 SETTLING TIME

The photos of Figures 26 and 27 show the dynamic response of the AD744 while operating in the settling time test circuit of Figure 25. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD744 under test, is clamped, amplified by op amp A2 and then clamped again.

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4 V overload quickly enough to allow accurate measurement of the AD744's 500 ns settling time. Amplifier A2 is a very high-speed FET-input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD744 under test.

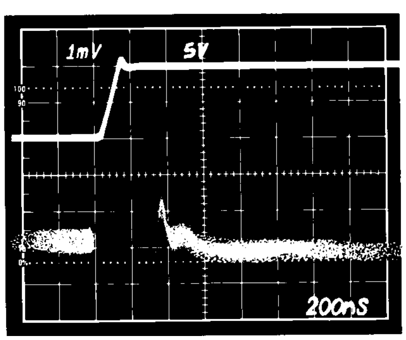


Figure 26. Settling Characteristics 0 to +10 V Step
Upper Trace: Output of AD744 Under Test (5 V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

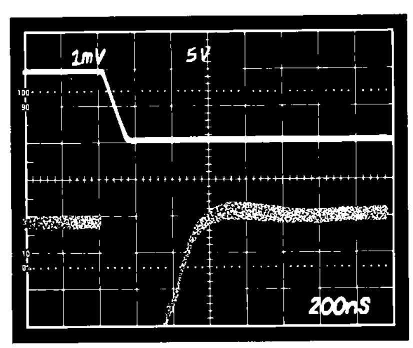


Figure 27. Settling Characteristics 0 to –10 V Step
Upper Trace: Output of AD744 Under Test (5 V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

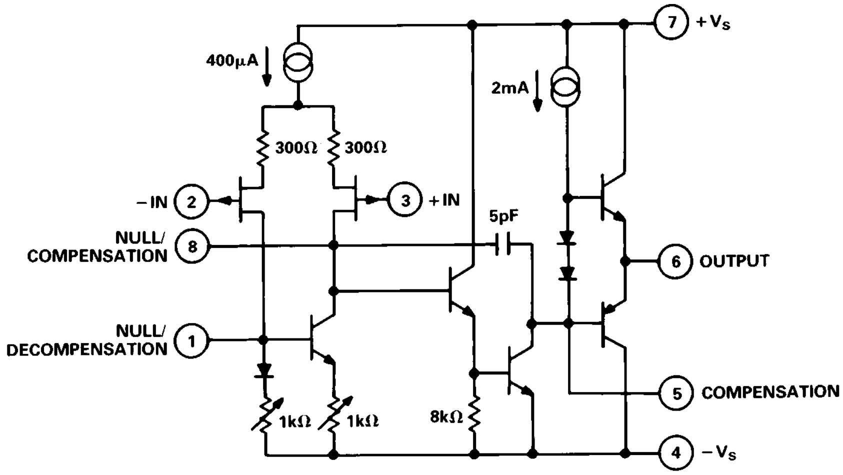


Figure 28. AD744 Simplified Schematic

EXTERNAL FREQUENCY COMPENSATION

Even though the AD744 is useable without compensation in most applications, it may be externally compensated for even more flexibility. This is accomplished by connecting a capacitor between Pins 5 and 8. Figure 28, a simplified schematic of the AD744, shows where this capacitor is connected. This feature is useful because it allows the AD744 to be used as a unity gain voltage follower. It also enables the amplifier to drive capacitive loads up to 2000 pF and greater.

The slew rate and gain bandwidth product of the AD744 are inversely proportional to the value of the compensation capacitor, C_{COMP}. Therefore, when trying to maximize the speed of the amplifier, the value of C_{COMP} should be minimized. C_{COMP} can also be used to slow the amplifier to a point where the slew rate is perfectly symmetrical and well controlled. Figure 29 summarizes the effect of external compensation on slew rate and bandwidth.

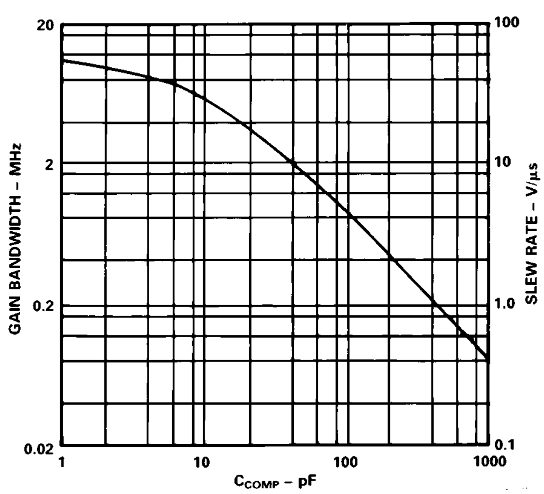


Figure 29. Gain Bandwidth and Slew Rate vs. C_{COMP}

The following section provides tables to show what C_{COMP} values will provide the necessary compensation for given circuit configurations and capacitive loads. In each case, the recommended C_{COMP} is a minimum value. A larger C_{COMP} can always be used, but slew rate and bandwidth performance will be degraded.

Figure 30 shows the AD744 configured as a unity gain voltage follower. In this case, a minimum compensation capacitor of 5 pF is necessary for stable operation. Larger compensation capacitors can be used for driving larger capacitive loads. Table I outlines recommended minimum values for C_{COMP} based on the desired capacitive load. It also gives the slew rate and bandwidth that will be achieved for each case.

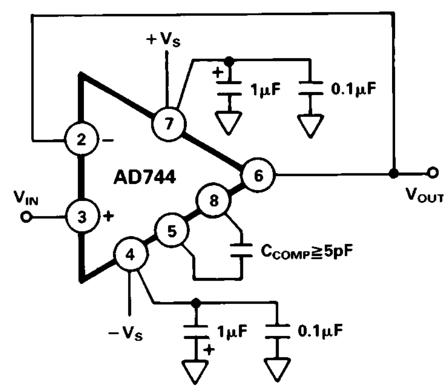


Figure 30. AD744 Connected as a Unity Gain Voltage Follower

Table I. Recommended Values of C_{COMP} vs. Various Capacitive Loads

Gain	Max C_{LOAD} (pF)	C_{COMP} (pF)	Slew Rate (V/µs)	–3 dB Bandwidth (MHz)
1	50	5	37	6.5
1	150	10	25	4.3
1	2000	25	12.5	2.0

Figures 31 and 32 show the AD744 as a voltage follower with gain and as an inverting amplifier. In these cases, external compensation is not necessary for stable operation. However, compensation may be applied to drive capacitive loads above 50 pF. Table II gives recommended C_{COMP} values, along with expected slew rates and bandwidths for a variety of load conditions and gains for the circuits in Figures 31 and 32.

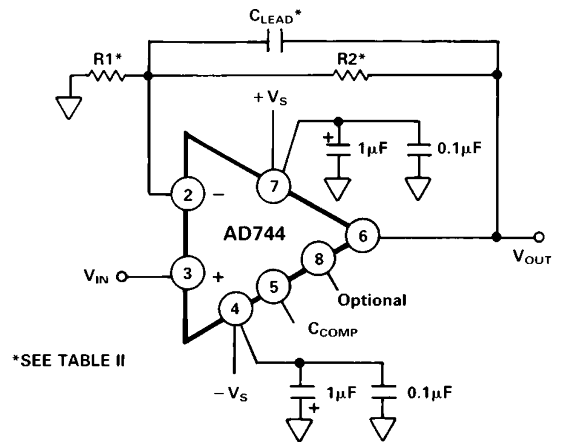


Figure 31. AD744 Connected as a Voltage Follower Operating at Gains of 2 or Greater

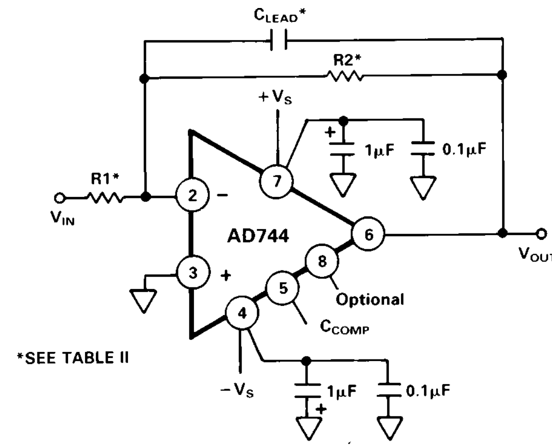


Figure 32. AD744 Connected as an Inverting Amplifier Operating at Gains of 1 or Greater

Table II. Recommended Values of C_{COMP} vs. Various Load Conditions for the Circuits of Figures 31 and 32.

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	Max C_{LOAD} (pF)	C_{COMP} (pF)	C_{LEAD} (pF)	Slew Rate (V/μs)	–3dB Bandwidth (MHz)
4.99 k	4.99 k	2	1	50	0	7	75	2.5**
4.99 k	4.99 k	2	1	150	5	7	37	2.3**
4.99 k	4.99 k	2	1	1000	20	–	14	1.2
4.99 k	4.99 k	2	1	>2000	25	–	12.5*	1.0
499 Ω	4.99 k	11	10	270	0	–	75	1.2
499 Ω	4.99 k	11	10	390	2	–	50	0.85
499 Ω	4.99 k	11	10	1000	5	–	37*	0.60

*Into large capacitive loads the AD744's 25 mA output current limit sets the slew rate of the amplifier, in V/μs, equal to 0.025 amps divided by the value of C_{LOAD} in μF. Slew rate is specified into rated max C_{LOAD} except for cases marked *, which are specified with a 50 pF. load.

**Bandwidth with C_{LEAD} adjusted for minimum settling time.

Using Decompensation to Extend the Gain Bandwidth Product

When the AD744 is used in applications where the closed-loop gain is greater than 10, gain bandwidth product may be enhanced by connecting a small capacitor between Pins 1 and 5 (Figure 33). At low frequencies, this capacitor cancels the effects of the chip's internal compensation capacitor, C_{COMP}, effectively decompensating the amplifier.

Due to manufacturing variations in the value of the internal C_{COMP}, it is recommended that the amplifier's response be optimized for the desired gain by using a 2 to 10 pF trimmer capacitor rather than using a fixed value.

Table III. Performance Summary for the Circuit of Figure 33

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	–3dB Bandwidth	Gain/BW Product
1 k	10 k	11	10	2.5 MHz	25 MHz
100	10 k	101	100	760 kHz	76 MHz
100	100 k	1001	1000	225 kHz	225 MHz

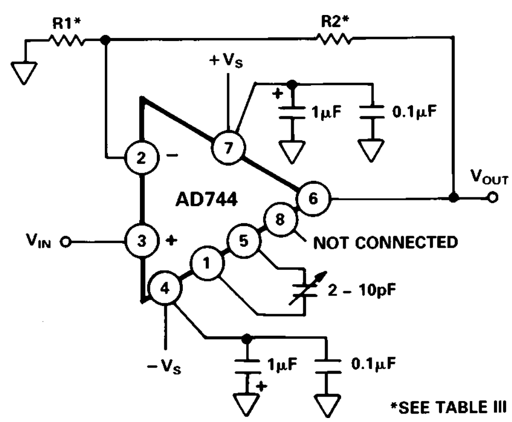


Figure 33. Using the Decompensation Connection to Extend Gain Bandwidth

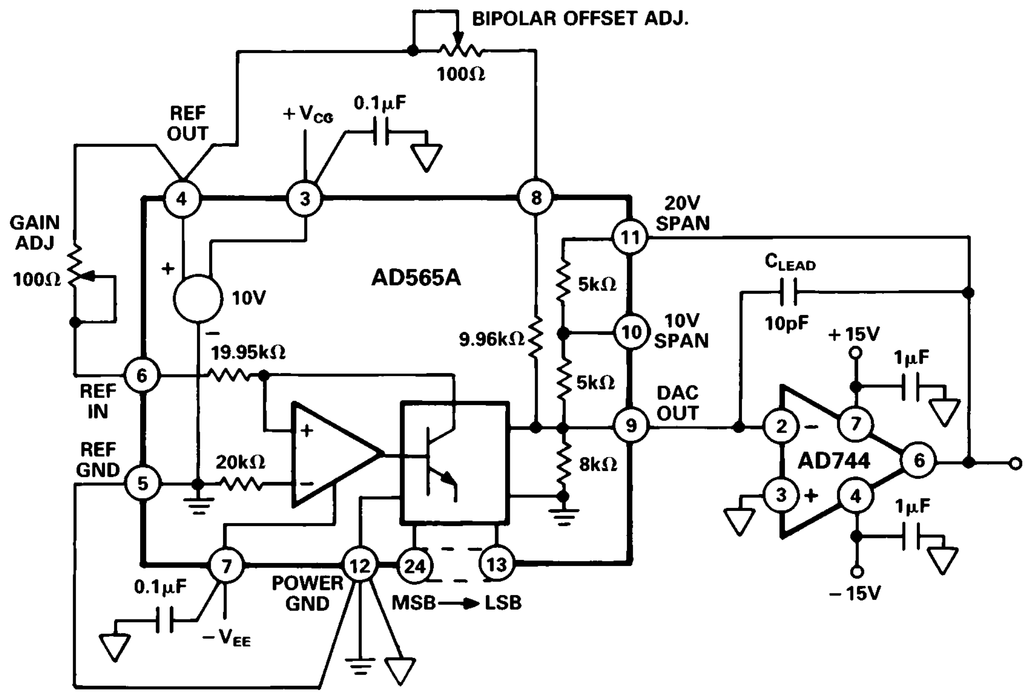


Figure 34. ±10 V Voltage Output Bipolar DAC Using the AD744 as an Output Buffer

HIGH-SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

Digital-to-analog converters which use bipolar transistors to switch currents into (or out of) their outputs can achieve very fast settling times. The AD565A, for example, is specified to settle to 12 bits in less than 250 ns, with a current output. However, in many applications, a voltage output is desirable, and it would be useful – perhaps essential – that this I-to-V conversion be accomplished without increasing the settling time or without degrading the accuracy of the DAC.

Figure 34 is a schematic of an AD565A DAC using an AD744 output buffer. The 10 pF C_{LEAD} capacitor compensates for the DAC's output capacitance, plus the 5.5 pF amplifier input capacitance.

Figure 35 is an oscilloscope photo of the AD744's output voltage with a +10 V to 0 V step applied; this corresponds to an all "1s" to all "0s" code change on the DAC. Since the DAC is connected in the 20 V span mode, 1 LSB is equal to 4.88 mV. Output settling time for the AD565/AD744 combination is less than 500 ns to within a 2.44 mV, 1/2 LSB error band.

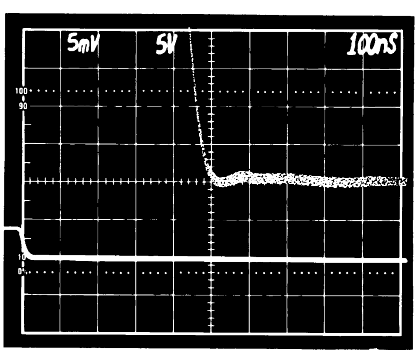


Figure 35. Upper Trace: AD744 Output Voltage for a +10 V to 0 V Step, Scale: 5 mV/div. Lower Trace: Logic Input Signal, Scale: 5 V/div.

A HIGH-SPEED, 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 36 can provide a range of gains from unity up to 1000 and higher. The circuit bandwidth is 4 MHz at a gain of 1 and 750 kHz at a gain of 10; settling time for the entire circuit is less than 2 μs to within 0.01% for a 10 V step, (G = 10).

While the AD744 is not stable with 100% negative feedback (as when connected as a standard voltage follower), phase margin and therefore stability at unity gain may be increased to an acceptable level by placing the parallel combination of a resistor and a small lead capacitor between each amplifier's output and its inverting input terminal.

The only penalty associated with this method is a small bandwidth reduction at low gains. The optimum value for C_{LEAD} may be determined from the graph of Figure 41. This technique can be used in the circuit of Figure 36 to achieve stable operation at gains from unity to over 1000.

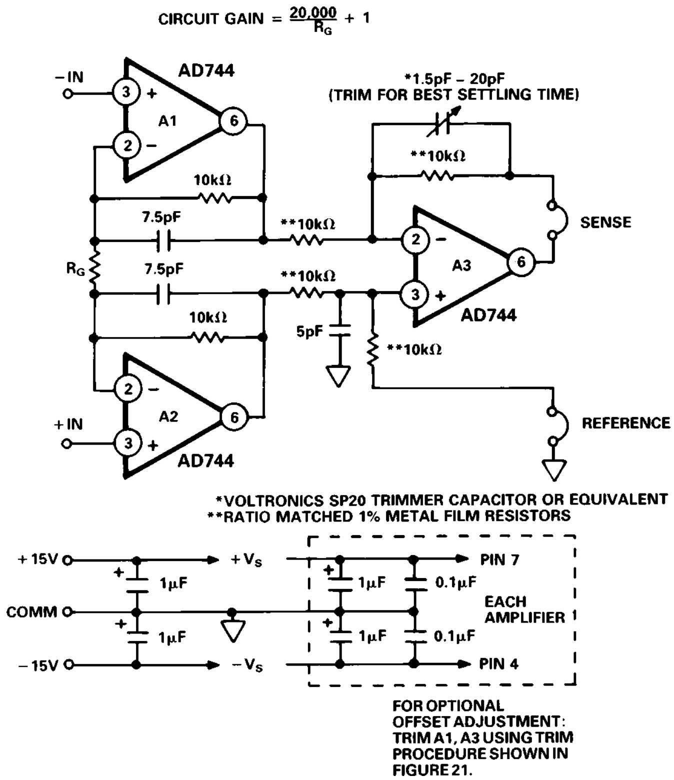


Figure 36. A High Performance, 3 Op Amp Instrumentation Amplifier Circuit

Table IV. Performance Summary for the 3 Op Amp Instrumentation Amplifier Circuit

Gain	RG	Bandwidth	T Settle (0.01%)
1	NC	3.5 MHz	1.5 µs
2	20 kΩ	2.5 MHz	1.0 µs
10	2.22 kΩ	1 MHz	2 µs
100	202 Ω	290 kHz	5 µs

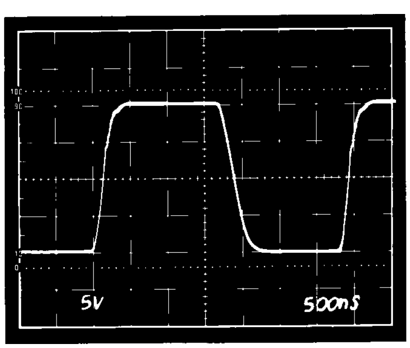


Figure 37. The Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 1, l Horizontal Scale: 0.5 µV/div., Vertical Scale: 5 V/div. (Gain= 10)

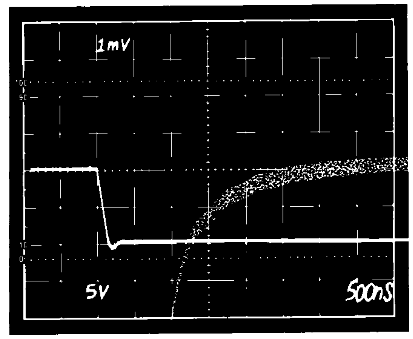


Figure 38. Settling Time of the 3 Op Amp Instrumentation Amplifier. Horizontal Scale: 500 ns/div., Vertical Scale, Pulse Input: 5 V/div., Output Settling: 1 mV/div.

Minimizing Settling Time in Real-World Applications

An amplifier with a "single pole" or "ideal" integrator open-loop frequency response will achieve the minimum possible settling time for any given unity-gain bandwidth. However, when this "ideal" amplifier is used in a practical circuit, the actual settling time is increased above the minimum value because of added time constants which are introduced due to additional capacitance on the amplifier's summing junction. The following discussion will explain how to minimize this increase in settling time by the selection of the proper value for feedback capacitor, C_L.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency, f_O, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 39. This circuit models an op amp connected as an I-to-V converter.

Equation 1 would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects. Even considering these effects, the fine scale settling to <0.1% will be determined by the op amp's small signal behavior.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_L + C_X)}{2\pi F_O} s^2 + \left(\frac{G_N}{2\pi F_O} + RC_L\right) s + 1}$$

Where F_O = the op amp's unity gain crossover frequency

$$G_N = \text{the "noise" gain of the circuit} \left(1 + \frac{R}{R_O}\right)$$

This Equation May Then Be Solved for C_L:

Equation 2.

$$C_L = \frac{2 - G_N}{R 2\pi F_O} + \frac{2\sqrt{RC_X 2\pi F_O + (1 - G_N)}}{R 2\pi F_O}$$

In these equations, capacitance C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling an I-to-V converter application, the Norton equivalent circuit of Figure 39 can be used directly. Capacitance C_X is the total capacitance of the output of the current source plus the

input capacitance of the op amp, which includes any stray capacitance at the op amp's input.

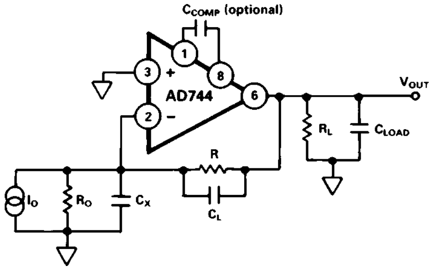


Figure 39. A Simplified Model of the AD744 Used as a Current-to-Voltage Converter

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier model of Figure 40 is created. Here capacitor C_X represents the input capacitance of the AD744 (5.5 pF) plus any stray capacitance due to wiring and the type of IC package employed.

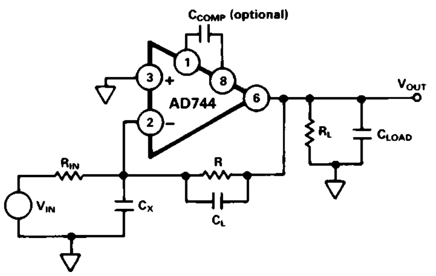


Figure 40. A Simplified Model of the AD744 Used as an Inverting Amplifier

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp's output. If the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose the correct value for a small capacitor, C_L, which will optimize amplifier response. If the value of C_X is not known, C_L should be a variable capacitor.

As an aid to the designer, the optimum value of C_L for one specific amplifier connection can be determined from the graph of Figure 41. This graph has been produced for the case where the AD744 is connected as in Figures 39 and 40 with a practical minimum value for C_{STRAY} of 2 pF and a total C_X value of 7.5 pF.

The approximate value of C_L can be determined for almost any application by solving Equation 2. For example, the AD565/ AD744 circuit of Figure 34 constrains all the variables of Equation 2 (G_N = 3.25, R = 10 kΩ, F_O = 13 MHz, and C_X = 32.5 pF) Therefore, under these conditions, C_L= 10.5 pF.

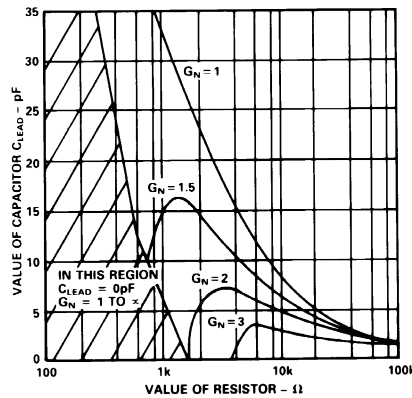
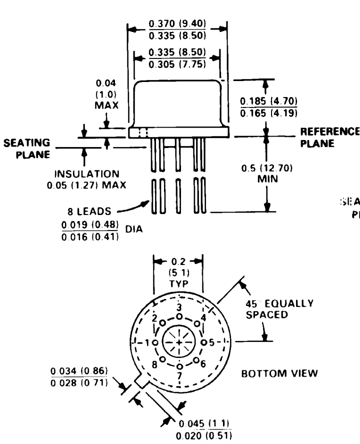


Figure 41. Practical Values of C_L vs. Resistance of R for Various Amplifier Noise Gains

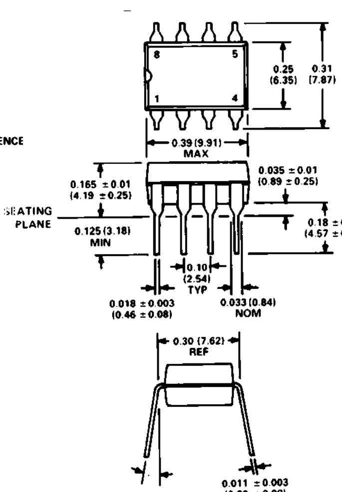
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

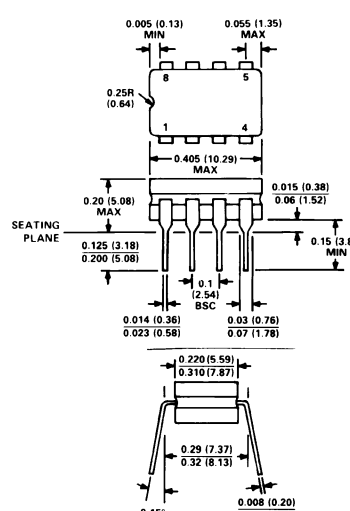
TO-99 (H) Package



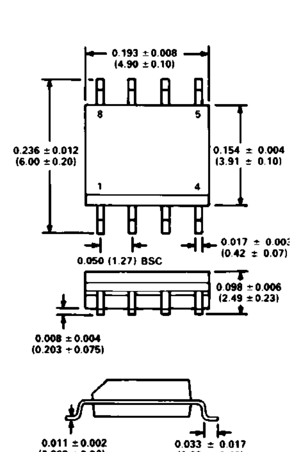
Mini-DIP (N) Package



Cerdip (Q) Package



Small Outline (R) Package



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